M3V Series

9x14 mm, 3.3 Volt, HCMOS/TTL, VCXO





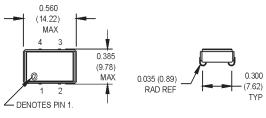


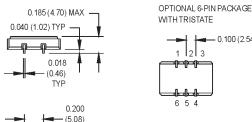


- 0.100 (2.54) TYP

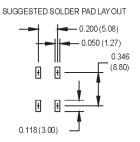
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- HCMOS/TTL output to 160 MHz and excellent jitter (2.1 ps typ.) in a SMT package
- Phase-Locked Loops (PLL's), Clock Recovery, Reference Signal Tracking, Synthesizers, Frequency Modulation/Demodulation



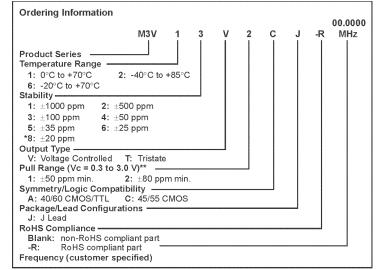






Pin Connections

FUNCTION	4 Pin Pkg.	6 Pin Pkg.	
Control Voltage	1	1	
Tristate		2	
Circuit/Case Ground	2	3	
Output	3	4	
N/C		5	
+Vdd	4	6	



^{*}Contact factory for availability.
**Other pull ranges available. Contact factory.
M3005Sxxx - Contact factory for datasheet.

	PARAMETER	Symbol	Min.	Тур.	Max.	Units	Condition/Notes		
	Frequency Range	F	1.544		160	MHz	See Note 1		
	Operating Temperature	T _A	(See ordering information)						
	Storage Temperature	Ts	-55		+125	°C			
	Frequency Stability	ΔF/F		(See orde	ring informa				
	Aging 1st Year		-3/-5		+3/+5	ppm	<52 MHz / >=52MHz		
	Thereafter (per year)		-1/-2	(0)	+1/+2	ppm	<52 MHz / >=52MHz		
	Pullability/APR			<u> </u>	ring informa	Over Control Voltage			
	Control Voltage	Vc	0.3	1.65	3.0	V			
	Linearity	<u> </u>			10	%	Positive Monotonic Slope		
	Modulation Bandwidth	Fm	10		$\overline{}$	kHz			
2	Input Impedance	Zin	50k			Ohms			
Ϊ́	Input Voltage	Vdd	3.135	3.3	3.465	V			
Electrical Specification	Input Current	Idd			20 55 65	mA mA mA	1.544 to 24 MHz 24.001 to 96 MHz 96.001 to 160 MHz		
S	Output Type						HCMOS/TTL		
a	Load						See Note 2		
Electric	1.544 to 60 MHz 60.001 to 160 MHz			10 T 5 TT					
1"	Symmetry (Duty Cycle)		(See ordering information)				See Note 3		
	Logic "1" Level	Voh	90% Vdc			V	HCMOS Load		
			Vdd -0.5	<u> </u>	-	V	TTL Load		
	Logic "0" Level	Vol			10% Vdd 0.5	V	HCMOS Load		
	Rise/Fall Time	Tr/Tf		3	10	ns	See Note 4		
	Tristate Function	11/11	Input Loc				See Note 4		
	instate runction		Input Logic "1" or floating: output active Input Logic "0": output disables to high-Z						
	Start up Time				10	ms			
	Phase Jitter @ 155.52 MHz	φЈ		3	5	ps RMS	Integrated 12 kHz - 20 MHz		
	Phase Noise (Typical) @155.52 MHz	10 Hz -60	100 H z -90	1 kHz -112	10 kH 2	2 100 kHz -120	Offset from carrier dBc/Hz		
Ital	Mechanical Shock	Per MIL-STD-202, Method 213, Condition C (100 g's, 6 mS duration, ½ sinewave)							
Jen	Vibration	Per MIL-STD-202, Method 201 & 204 (10 g's from 10-2000 Hz)							
Environmental	Hermeticity	Per MIL-STD-202, Method 112, (1x10-8 atm. cc/s of Helium)							
	Solderability	Per EIAJ-STD-002							
	Max Soldering Conditions	See solder profile, Figure 1							
	Frequencies above 70 MHz utilize a PLL design. Fundamental and PLL designs are available at other frequencies.								

- Frequencies above 70 MHz utilize a PLL design. Fundamental and PLL designs are available at other frequencies Contact factory for availability.
- 2. TTL load see load circuit diagram #1. HCMOS load see load circuit diagram #2.
- 3. Symmetry is measured at 1.4 V with TTL load, and at 50% Vdd with HCMOS load.
- 4. Rise/Fall times are measured between 0.5 V and 2.4 V with TTL load, and between 10% Vdd and 90% Vdd with HCMOS load.

MtronPTI reserves the right to make changes to the product(s) and service(s) described herein without notice. No liability is assumed as a result of their use or application.





